II. SPECIFICATION AMENDMENTS

Please cancel the present Abstract and substituted therefor a new abstract presented on a separate sheet enclosed herewith.

~~A digital serial interface is provided between a transmitting device (303) and a receiving device (304) for transmitting a serial sequence of data bits and a number of associated synchronization signals over a wired connection. The transmitting device comprises primary transmitter means (401) for converting a serial sequence of data bits into successive data signal levels in an output line (Vline+, Vline-). Said data signal levels are selected from a first group of levels. The transmitting device comprises also secondary transmitter means (403, 601, 602) for converting synchronization signals into synchronization signal levels on said output line. Said synchronization signal levels are selected from a second group of levels which consists of different levels than said first group of levels. The receiving device comprises primary receiver means (402, 801) that are responsive to a first group of signal levels. They are used for converting a sequence of successive data signal levels in an input line into a serial sequence of data bits. The receiving device comprises also secondary receiver means (404, 405, 802, 804) that are responsive to a second group of signal levels which consists of different levels than said first group of signal levels. They are used for converting synchronization signal levels in said input line into synchronization signals.~~

A digital serial interface connects a transmitting device with a receiving device for communicating both data bits and synchronization signals via the serial interface. The transmitting device include a primary transmitter for converting a serial sequence of the data bits into successive data signal levels, and further includes a secondary transmitter for converting synchronization signals into synchronization signal levels different from the levels employed for the data signals. The receiving device has a primary receiver for the data signal levels for converting a sequence of data signal levels into a serial sequence of data bits, and further includes a secondary receiver for the synchronization signal levels for converting synchronization signal levels into synchronization signals.

Please replace the paragraphs on page 6, lines 22 through line 24, as rewritten below:

~~Fig. 10 illustrates an apparatus according to a fourth embodiment of the invention and~~

~~Fig. 11 illustrates a voltage level diagram relating to Fig. 10.~~

Fig. 10 illustrates an apparatus according to a fourth embodiment of the invention,

Fig. 11 illustrates a voltage level diagram relating to Fig. 10, and

Fig. 12 illustrates use of an embodiment of the invention according to Fig. 4, 6, 8 or 10.
